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Description

IMPROVED PROCESS FOR FORMING A BURIED PLATE

BACKGROUND OF INVENTION

[0001] The invention relates to semiconductor processing, and more particularly to an improved method for forming a buried plate such as used in a trench capacitor of an advanced microelectronic device, e.g., a dynamic random access memory (DRAM).

[0002] A goal of the semiconductor industry is to increase the circuit density of integrated circuits ("ICs" or "chips"), most often by decreasing the size of individual devices and circuit elements of a chip. Trench capacitors are used in some types of DRAMs for storing data bits. Often, increasing the circuit density of such DRAMs requires reducing the size of the trench capacitor, which, in turn, requires reducing the area of the chip occupied by the trench capacitor. Achieving such reduction in surface area is not straightforward, because different components of

the storage capacitor do not scale at the same rate, and some components cannot be scaled below a certain size. It would be desirable to provide a process of forming a trench capacitor which helps maintain the lateral dimensions of the trench capacitor within the tolerances at the surface of the chip required to achieve further reductions.

[0003] The fabrication of a trench capacitor begins by etching an opening in a semiconductor substrate. A trench capacitor is typically formed by a series of process steps, starting by etching a deep trench in a semiconductor region of a substrate. A patterned pad stack is generally provided on the substrate to define a window through which the opening is to be etched.

[0004] The trench capacitor is a plate capacitor, having as a first plate a "buried plate", which is a charge-containing region in the semiconductor substrate adjacent to the sidewall of the trench. A second plate of the capacitor is provided as a "node electrode", separated from the buried plate by a thin "node dielectric." The buried plate is typically disposed adjacent to only a lower portion of the trench, while an isolation collar is provided in the upper portion of the trench to isolate the trench capacitor from other nearby devices such as transistors. The buried plate is typically

formed by outdiffusion of dopants from a dopant source into the lower portion. Typically, the dopant source is one that provides dopants, such as arsenic-doped silicate oxide, i.e., arsenic-doped glass (ASG). The dopant source is deposited to cover the sidewalls and bottom of the trench, such as through a low-pressure chemical vapor deposition (LPCVD) process. Thereafter, an annealing process is conducted to drive the dopants into the adjacent areas of the substrate to form the buried plate.

[0005] Unfortunately, conventional processing using ASG as a dopant source is not ideal. The ASG deposition tends to oxidize the semiconductor material at the sidewall of the deep trench. The ASG deposition also tends to cause dopant diffusion into the semiconductor material beyond the oxidized layer that forms at the semiconductor surface. These problems are illustrated with reference to Figure 1.

[0006] Figure 1 is a cross-sectional view illustrating a stage in the formation of a buried plate for a trench capacitor according to a prior art process. As shown in Figure 1, a trench 105 is vertically etched into the semiconductor substrate 100 through an opening 115 in a pad stack 130. The sidewall 110 of the trench represents the edge of the

semiconductor substrate, as stands after first etching the trench 105, before subsequent processes are performed. Illustratively, a layer 112 of ASG is deposited onto the sidewall 110 and bottom 145 of the trench 105 as a source of dopant material for later forming the buried plate. However, as a result of the deposition of the ASG, an oxide layer 150 forms due to the oxidation of the semiconductor substrate adjacent to the original trench sidewall 110. The oxide region 150 extends outwardly from the original trench sidewall 110 to a post-oxidation sidewall 140, thus widening the lateral dimension of the trench to the sidewall 140. The widening of the upper portion 180 of the trench is undesirable, because it negatively impacts the overlay tolerance. In addition, arsenic outdiffuses into the region 190 of the substrate adjacent to the oxidized region 150 during the ASG deposition process. Doping the upper trench portion 180 is undesirable because it increases the device leakage current and negatively impacts device performance.

[0007] Figure 2 illustrates a subsequent stage in the conventional process of forming a buried plate, after a dopant drive-in anneal has been conducted. As shown, a buried plate 102 is disposed in the substrate surrounding a lower portion

170 of the sidewall of the trench 105. Illustratively, a layer 200 of an undoped oxide is disposed as a cap to protect the upper portion 180 of the trench sidewall from unwanted doping during the anneal process to drive dopants diffusing into the lower portion 170 of the trench. The cap layer 200 is formed after the undesired oxide 150 (Figure 1) and the ASG layer have been removed from the upper portion 180 of the post-oxidation sidewall 140 of the widened trench.

[0008] Figure 3 illustrates a further stage in fabrication, after a buried plate 102 has been formed. The trench with widened upper portion 180 is further illustrated in Figure 3 as an increase in a lateral dimension 310, as measured by the spacing bounded by the post-oxidation trench sidewall 140. This increased dimension 310 is shown in relation to the original lateral dimension 305 of the trench, as represented by the original location 210 of the trench sidewall 110 (Figure 1).

[0009] The two problems of trench widening and diffusion of arsenic into the substrate adjacent to the upper portion of the trench negatively impact the performance of the trench capacitor and the ability to maintain process tolerances. Both problems are due to the direct deposition of

dopant source material (e.g., ASG) on the sidewall of the semiconductor substrate. Accordingly, a new method is desired to address the foregoing concerns.

Summary of Invention

[0010] A method is provided for forming a buried plate region in a substrate. A trench is formed in a semiconductor substrate, the trench having a trench sidewall, the sidewall including an upper portion, and a lower portion disposed below the upper portion. A liner is formed along the trench sidewall, and thereafter, a dopant source layer is formed over the liner in the lower portion of the trench. The liner prevents the upper portion of trench sidewall from being oxidized and doped. Buried plate is then formed by performing an anneal process to drive a dopant from the dopant source layer into the semiconductor substrate adjacent to the lower portion of the trench sidewall.

Brief Description of Drawings

[0011] Figures 1 through 3 are a cross-sectional views illustrating stages in the fabrication of a trench capacitor according to a prior art method; and

[0012] Figures 4 through 16 are cross-sectional views illustrating stages in the formation of a trench capacitor according to

embodiments of the invention.

Detailed Description

[0013] The embodiments of the invention described herein address the problems of the prior art, including the diffusion of a dopant into undesired areas and the undesired widening of the upper portion of the trench. In one embodiment, a liner is formed on an exposed surface of the semiconductor substrate at the trench sidewall prior to depositing a dopant source layer such as ASG. During the dopant source layer deposition, the liner functions as a diffusion barrier to prevent arsenic from diffusing into the semiconductor material at the upper portion of the trench. The liner also prevents the semiconductor substrate present at the trench sidewall from being oxidized during that deposition. During subsequent annealing, the liner loses its barrier function, allowing the dopant to outdiffuse into the semiconductor material adjacent the lower portion of the trench to form the buried plate. Further steps are performed to complete the trench capacitor.

[0014] Figures 4 through 16 illustrate stages in processing according to an embodiment of the invention. Figures 4 through 6 illustrate a process of patterning a trench. Illustratively, in this process, the trench is patterned in a

semiconductor substrate 400, which typically consists essentially of p-type doped silicon. Alternatively, the substrate has a semiconductor-on-insulator type structure, e.g., is a silicon-on-insulator (SOI) substrate. Other suitable alternative types of substrates include germanium, silicon germanium, silicon carbide, strained silicon, and those consisting essentially of one or more compound semiconductors having a composition defined by the formula $Al_{X1}Ga_{X2}In_{X3}As_{Y1}P_{Y2}N_{Y3}Sb_{Y4}$, where X1, X2, X3, Y1, Y2, Y3, and Y4 represent relative proportions, each greater than or equal to zero and X1+X2+X3+Y1+Y2+Y3+Y4=1 (1 being the total relative mole quantity). Other suitable substrates have a composition $Zn_{A1}Cd_{A2}Se_{B1}Te_{B2}$, where A1, A2, B1, and B2 are relative proportions each greater than or equal to zero and A1+A2+B1+B2=1 (1 being a total mole quantity).

[0015] A variety of methods may be utilized to form the deep trench. Typically, a mask layer is first formed and patterned on the substrate, being comprised of a material less susceptible to etching, such as a hardmask layer of silicon oxide and/or silicon nitride or other material. Figure 4 shows one embodiment in which an oxide layer 405 functions as a hardmask layer, disposed over a pad stack

430 having a nitride layer 420 and an optional oxide layer 410. The oxide layer 410 is formed between the pad nitride layer 420 and the semiconductor substrate 400 as a buffer layer to improve the adhesion of the pad nitride layer 420 and to reduce the interface stress.

[0016] As shown in the cross-sectional depiction of Figure 5, the hardmask layer 405 is patterned and etched to create an opening 500 through which the trench will then be formed in the semiconductor substrate. Patterning can be done by forming a photoresist layer (not shown) and developed by any suitable process such as optical lithography, electron beam lithography, x-ray lithography, and ion beam lithography. The hardmask layer 405, along with the underlying pad stack 430 can then be etched selective to the photoresist using any conventional etch process, for example, reactive ion etch (RIE). The photoresist is stripped after forming opening the hardmask or after opening the hardmask and the underlying pad stack.

[0017] Referring to Figure 6, the substrate 400 then is etched by any suitable process such as RIE to form deep trench 600. The remaining the hardmask layer is stripped after forming the deep trench. The deep trench has a small width, typically ranging from 90 nm to 150 nm according to the

current generation of semiconductor devices. The deep trench is etched to a depth ranging between about 2 microns (μm) and 10 μm. Etching defines a trench 600 having a sidewall 620, and a bottom 610. In one embodiment as illustrated in Figure 6, the trench 600 is patterned in a manner that aligns an edge 630 of the pad stack 430 to the sidewall 620 of the trench 600. Hereinafter, references generally to the trench sidewall and to the lower portion of the trench sidewall shall be understood to include the trench bottom 610 as well.

[0018] Referring to Figure 7, a liner 700 is formed along the trench sidewall 620. The liner includes a material that functions as a diffusion barrier to prevent the outdiffusion of a dopant into the semiconductor substrate adjacent the trench during a subsequent deposition of a dopant source layer However, during a still later high temperature anneal, the liner loses its function as a diffusion barrier, allowing the dopant to outdiffuse from the dopant source layer through the liner into the silicon to form the buried plate. The liner will also protect the sidewall of the trench from being oxidized during the dopant source material deposition. Preferably, the liner comprises of a nitride formed thermally by a controlled nitridation of the semi-

conductor material present at the trench sidewall. Accordingly, a liner including silicon nitride is formed by the nitridation when the substrate is predominantly a silicon substrate. Preferably, the thickness of such thermal nitride is ranging from 5 angstroms (Å) to 20 Å and more preferably from 7 Å to 10 Å. Alternatively, a thermal oxide is suitable, such as formed thermally by a controlled oxidation of the semiconductor material present at the trench sidewall. When the substrate is predominantly a silicon substrate, the resulting liner includes silicon oxide. The preferred thickness of the thermal oxide ranges from 10 Å to 50 Å and more preferably from 15 Å to 25 Å. Other suitable liner materials include silicon carbide and metal silicides, etc., formed by thermal growth or deposition.

[0019] Figure 8 illustrates a variation in which the liner 800 is deposited onto the sidewall 620 of the trench, rather than being formed by thermal nitridation or thermal oxidation. For example, the liner 800 can be formed by controlled LPCVD (low pressure chemical vapor deposition) or atomic layer deposition (ALD). In such case, the liner 800 extends over the pad stack 430. As a deposited liner, a layer of silicon nitride is suitable, having a thickness of between about 7 Å and 10 Å. Otherwise, a layer of silicon oxide

having a thickness of about 20 Å can be deposited. Alternatively, any of the liner materials discussed above is suitable as liners. Hereinafter, all references to the liner 700 are to a liner as formed by local reaction of the semiconductor material, as described with reference to Figure 7, with the understanding that a deposited liner 800 as described relative to Figure 8 could be used in its place.

[0020] Figure 9 illustrates a subsequent stage of processing in which a dopant source layer 900 is conformally deposited in the trench 600. The dopant source layer is typically ASG, having arsenic as an n-type dopant, although phosphosilicate glass (PSG) could be used instead, if processing conditions and results to be achieved permit. The dopant source layer 900 includes an n-type dopant for work function matching when used in trench capacitors connected in a typical arrangement to n-type FETs (NFETs) of an array of NFETs. Alternatively, a p-type dopant such as boron can be used when the capacitor requires a different work function, or for other purposes. In a typical dynamic random access memory (DRAM), trench capacitors connect to an array of NFETs. In such case, an n-type dopant source layer such as ASG is required to form the buried plate.

[0021] The deposition of the ASG layer 900 is illustratively performed by LPCVD, CVD (chemical vapor deposition), PECVD (plasma enhanced CVD), atomic layer deposition (ALD), or other suitable method. Preferably, low-pressure chemical vapor deposition (LPCVD) is used to deposit one or more relatively thin, high quality films. In a preferred embodiment, the ASG deposition is conducted by LPCVD at 700 °C for about 60 minutes, resulting in layer having a thickness of about 150 Å on the trench sidewall.

[0022] When the ASG layer 900 is deposited, the liner 700 acts as a diffusion barrier to suppress undesired outdiffusion of dopants into the semiconductor substrate. In addition, the liner 700 functions as a barrier during the ASG deposition to protect against undesired oxidation of the semiconductor substrate adjacent to the trench sidewall 620.

[0023] Referring to Figure 10, after the deposition of the ASG layer 900, a filler material 1000, such as a photoresist, (hereinafter "resist") is deposited in the trench. Thereafter, the resist is recessed to a predetermined level, as by a timed etch, e.g. reactive ion etch (RIE), to define an upper portion 1020 and a lower portion 1010 of the trench sidewall, as illustrated in the cross-sectional view of Figure 10. Alternatively, polysilicon can be deposited and re-

cessed to fulfill this function. The level 1030 to which the resist is recessed defines a lower portion 1010 of the sidewall of the trench on which the capacitor will be formed later, and an upper portion 1020 of the trench sidewall to be reserved for another purpose.

[0024] As shown in Figure 11, the ASG layer 900 is removed from the upper portion 1020 of the trench sidewall, while the ASG layer 900 and liner 700 remain in place along the lower portion 1010, where covered by the resist 1000. The liner 700 may or may not be removed along with the ASG layer 900 from the upper portion 1020 at this stage. Figure 11 shows a case in which the liner 700 is also removed from the upper portion 1020. Thereafter, Figure 12 illustrates a subsequent stage in which the resist is removed from the trench, leaving the ASG layer 900 and liner 700 in place along the lower portion 1010 of the trench sidewall.

[0025] Thereafter, as shown in Figure 13, a cap layer 1300 is deposited to cover the ASG layer 900 and liner 700 still present along the lower portion 1010 of the trench sidewall, as well as covering the exposed silicon along the upper portion 1020. As the cap layer 1300 is deposited conformally, it typically covers the pad stack 430, as well. The

cap layer 1300 is preferably an undoped oxide, which can be deposited by any suitable process, preferably by LPCVD, or PECVD.

[0026] Next, referring to Figure 14, a drive-in anneal is conducted to form the buried plate 1400. The anneal is performed at a temperature ranging from 900 °C to 1150 °C, and preferably from 1000 °C to 1100 °C, and more preferably at 1050 °C. The annealing environment may contain oxygen, nitrogen, hydrogen, argon, helium, or any combination of these. During such anneal, the cap layer 1300 covers the substrate 400 adjacent to the upper portion 1020 and protect the upper portion of the substrate from outdiffusion of the dopant from the dopant source layer 900. Since the drive-in anneal is performed at a relative high temperature, the dopant can diffuse through the liner 700 into the substrate 400 adjacent to the lower portion to form a counter doped region as a buried plate 1400.

[0027] Thereafter, with reference to Figure 15, the cap layer, ASG layer and liner are stripped, leaving the doped buried plate 1400 in the substrate adjacent to the lower portion 1010. At this point of processing, little, if any, widening of the trench has occurred in the upper portion 1020. With

the liner, the upper portion has been spared from undesired oxidation and diffusion of dopants therein during the deposition of the ASG layer. Otherwise, excessive oxidation of the substrate 400 adjacent to the upper portion might have resulted in undesired widening of the trench after the removing the formed oxide.

[0028] Figure 16 illustrates a stage of processing after further steps have been performed to complete a trench capacitor 1600 therein and a vertical transistor 1650 disposed above the trench capacitor 1600. As shown in Figure 16, the trench capacitor 1600 includes the buried plate 1400, a node dielectric 1610 formed on the sidewall 1605 of the silicon where the buried plate 1400 is located, and a node electrode 1620 disposed on the opposite side of the node dielectric 1610 from the buried plate 1400.

[0029] The formation of the vertical transistor 1650 along the upper portion 1020 of the trench sidewall is only illustrative. Many other structures and ways of forming transistors which connect to the trench capacitor are possible. In the example shown in Figure 16, the trench capacitor 1600 is separated from the vertical transistor by an isolation collar 1640 formed on a part of the upper portion of the trench sidewall. The vertical transistor includes a gate

conductor 1643, a gate dielectric 1645 and a channel region 1630. The channel region 1630 allows current to pass only when the gate conductor 1643 is biased at an appropriate voltage. The gate conductor 1643 is isolated from the node electrode 1620 by a trench top oxide 1660. The vertical transistor 1650 is electrically connected to the node electrode 1620 by an n-type buried strap outdiffusion 1670 formed in the silicon adjacent to the gate dielectric 1645, the trench top oxide 1660 and the node electrode 1620. A drain region 1647 is disposed above the channel region 1630.

[0030] Alternatively, instead of a vertical transistor, a planar transistor can be formed which connects to the trench capacitor 1600. Those skilled in the art will understand the known processes which can be used to form such planar transistor. Alternatively, the trench capacitor 1600 can be simply connected to circuitry of the chip, such as for use in providing a source of local capacitance, e.g., for decoupling purposes.

[0031] Figure 17 illustrates a variation of the above-described embodiment, in which the trench is widened to a bottle shape, prior to completing the trench capacitor. In this case, a widened trench sidewall 1710 results. Widening

the trench enlarges the cylindrical volume of the trench, which increases the outer surface area of the cylinder on which the trench capacitor will be formed, thus increasing capacitance. At the same time, the critical dimension of the trench in the region of the upper portion 1020 is maintained acceptably within tolerances for the overlaying of subsequent processes.

[0032] Preferably, the lower portion 1010 of the trench is widened by laterally etching the semiconductor material present at the sidewall 1500 (Figure 15) of the trench by an etch process which is selective to more lightly doped semiconductor material. Such etch process proceeds more rapidly against the more highly doped semiconductor material present along the lower portion of the trench sidewall after the dopant drive-in. The result of etching is to produce a widened sidewall 1710 that is disposed to the outside of the former lower portion 1020 of the trench sidewall.

[0033] Alternatively, the lower portion is widened after forming a collar 1720 in the upper portion of the trench. In such case, the collar 1720 is formed by depositing a fill material (not shown) into the trench, recessing it to the level of the lower portion of the trench, and then depositing an

oxide layer, or otherwise oxidizing the trench sidewall in the upper portion 1020. The oxide layer and fill material are then removed from the lower portion 1010 of the trench, as by RIE. Thereafter, the semiconductor material present at the lower portion of the trench sidewall is etched, as by a timed isotropic etch, to widen the lateral dimension of the trench to the bottle shape.

[0034] Accordingly, the foregoing described embodiments of the invention address challenges of the prior art through use of a liner to reduce diffusion of a dopant into the silicon along the upper portion of the trench sidewall and to reduce widening of the upper portion due to unwanted oxidation.

[0035] While the invention has been described in accordance with certain preferred embodiments thereof, those skilled in the art will understand the many modifications and enhancements which can be made thereto without departing from the true scope and spirit of the invention, which is limited only by the claims appended below.